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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/092,089	03/05/2002	Keiji Kishine	10746/32	8474
7590 10/17/2005			EXAMINER	
KENYON & KENYON One Broadway New York, NY 10004			WONG, LINDA	
			ART UNIT	PAPER NUMBER
			2634	
DATE MAILED: 10/17/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/092,089

Applicant(s)

KISHINE ET AL.

Examiner

Linda Wong

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 8-11 is/are allowed.
- 6) ☒ Claim(s) 1,3,4 and 18 is/are rejected.
- 7) ☐ Claim(s) 5-7 and 12-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. **Claim 2** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 2 recites the limitation of a "M=KxL, L is a natural number". Although L is defined as a natural number, a description of L is not defined. Thus, it is unclear as to what L refers to. For example, claim 1 recites M number of demultiplexed signals. M is described as the number of signals outputted from the demultiplexor.

### *Claim Rejections - 35 USC § 102*

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1 and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Okamoto (US Patent No.: 5703511).
  - a. **Claim 1**, Okamoto discloses a clock and data recovery system in the form of a phase locked loop (PLL) comprising a voltage control oscillator (VCO) for outputting a clock signal of a frequency 1/K (Fig. 20, labels 625, 626, and 627), a delay circuit for delaying the input signal (Fig. 20, label 621), a demultiplexor for demultiplexing the input data signal into M demultiplexed signals (Fig. 19, label 64), a multiplexer for multiplexing the M demultiplexed signals (Fig. 19,

labels 10-bit parallel bit and 61) by a clock signal (Fig. 19, label 1 GHz), a phase comparator comprising phases of an output signal (Fig. 20, label 622), a lowpass filter (Fig. 20, label 624), wherein the clock/data recovery circuit outputs a clock signal generated by the VCO (Fig. 20, label Clock Output) and outputs M demultiplexed signals (Fig. 19, labels 10-Bit parallel data and 64).

- b. **Claim 18** inherits all the limitations of claim 1.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto (US Patent No.: 5703511).

- a. **Claim 3**, Okamoto discloses a second delay circuit, provided before the first delay circuit (Fig. 21, labels 631, and 630), another phase comparator, instead of the phase comparator, for comparing the phases of the first delay circuit and output from the multiplexer (Fig. 21, label 631,632 and Output of Mux 61) and comparing the output from the phase comparator and another clock. Although the other clock is not delayed, it would be obvious to one skilled in the art to delay the reference clock disclosed by Okamoto to ensure timing of the output

from the phase comparator and the reference clock matches so to eliminate errors caused when the timing between the two inputs are not.

4. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto (US Patent No.: 5703511) in view of Obana et al (US Patent No.: 5001711).
  - a. **Claim 4**, Although Okamoto does not disclose the components within the demultiplexer and multiplexer, Obana et al discloses a multiplexer/demultiplexer apparatus, wherein the demultiplexer comprises a first D-type flip-flop for receiving input data signal using a clock signal (Fig. 6A, labels 12, 22 and CKc), a second D-type flip flop for receiving input data signal by using a clock signal (Fig. 6A, labels 12, 22 and CKc), a multiplexer comprising a clock delay circuit (Fig. 6A, labels 13 and 44.736 and 1/7) and a selector for selecting one of the outputs out of the two d-type flip-flops (Fig. 6A, label 13). It would be obvious to one skilled in the art to incorporate a demultiplexer/multiplexer circuit as disclosed by Obana et al into Okamoto's invention to easily produce large scale integrated circuits. (Col. 1, lines 46-57)

***Allowable Subject Matter***

5. **Claims 5, 6,7,12-17** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. **Claims 8-11** are allowed over prior art.

Art Unit: 2634

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong



**STEPHEN CHIN**  
**SUPERVISORY PATENT EXAMINER**  
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